

WHAT IS CLAIMED IS:

1. A display device comprising:
a plurality of pixels disposed in a matrix configuration;
5 a plurality of gate lines extending in a direction; and
a driving circuit supplying a gate scanning signal to the gate lines, each of the pixels
being selected according to the gate scanning signal,
wherein at least one of the gate lines comprises a first gate line and a second gate line,
and a metal wiring connects the first and second gate lines and is located near an output portion
10 of the vertical driving circuit, the metal wiring being formed at a processing step different from a
processing step of forming the gate lines.

2. The display device of claim 1, wherein a distance between the first and second gate
lines is larger than 10 μm .

3. The display device of claim 1, wherein a distance between an edge of the first gate
line and a gate wiring in the output portion of the vertical driving circuit is larger than 10 μm , the
edge of the first gate line facing the gate wiring in the output portion.

4. The display device of claim 1, wherein the second gate line is connected to the
pixels.

5. The display device of claim 1, wherein the gate lines are made of molybdenum,
chrome, a molybdenum alloy or a chrome alloy.

6. The display device of claim 1, wherein the metal wiring is made of aluminum or an
aluminum alloy.

7. The display device of claim 1, wherein the metal wiring is disposed above the gate
lines.

8. A display device comprising:
a plurality of pixels disposed in a matrix configuration;
a plurality of gate lines extending in a row direction;
a plurality of date lines extending in a column direction;
5 a vertical driving circuit supplying a gate scanning signal to the gate lines; and
a horizontal driving circuit generating a drain scanning signal for controlling a timing of
supplying a video signal to the date lines,

wherein a gate wiring supplying a signal to at least two thin film transistors that are
disposed in the vertical driving circuit or in the horizontal driving circuit comprises at least two
10 wiring lines, and the wiring lines are connected by a metal wiring that is formed at a processing
step different from a processing step of forming the gate wiring.

9. The display device of claim 8, wherein each of the wiring lines is connected to only
one corresponding thin film transistor.

10. The display device of claim 8, further comprising another gate wiring connected to
at least one of the thin film transistors.

11. The display device of claim 8, wherein the gate wiring is configured to supply the
20 signal to more than two thin film transistors.

12. The display device of claim 8, wherein the metal wiring is disposed above the gate
wiring.

13. A display device comprising:
a plurality of pixels disposed in a matrix configuration;
a plurality of gate lines extending in a row direction;
a plurality of date lines extending in a column direction;
25 a vertical driving circuit supplying a gate scanning signal to the gate lines; and
a horizontal driving circuit generating a drain scanning signal for controlling a timing of
30 supplying a video signal to the date lines,

wherein a gate wiring supplying a signal directed to a plurality of active layers that are formed in the vertical driving circuit or in the horizontal driving circuit comprises a plurality of wiring lines, and the wiring lines are configured so as to be in direct contact with only one corresponding active layer and are connected by a metal wiring that is formed at a processing step different from a processing step of forming the gate wiring.

14. The display device of claim 13, further comprising another gate wiring supplying another signal directed to at least one of the active layers.

15. The display device of claim 13, wherein the gate wiring is configured to supply the signal to more than two active layers.

16. A display device comprising:
a plurality of pixels disposed in a matrix configuration;
a plurality of gate lines extending in a row direction;
a plurality of date lines extending in a column direction;
a vertical driving circuit supplying a gate scanning signal to the gate lines; and
a horizontal driving circuit generating a drain scanning signal for controlling a timing of supplying a video signal to the date lines;

wherein an active layer receiving a plurality signals from corresponding gate wirings and disposed in the vertical driving circuit or in the horizontal driving circuit comprises at least two active layer portions, and the active layer portions are connected by a metal wiring.

17. The display device of claim 16, wherein the active layer is configured to receive the signals form more than two gate wirings.

18. The display device of claim 16, wherein the active layer is configured to operate as part of a thin film transistor having a plurality of gates.

19. The display device of claim 16, wherein each of the active layer portions is configured to be in direct contact with only one corresponding gate wiring.

20. A display device comprising:

a plurality of pixels disposed in a matrix configuration;

a plurality of gate lines extending in a row direction;

5 a plurality of data lines extending in a column direction;

a vertical driving circuit supplying a gate scanning signal to a plurality of the gate lines;

and

a horizontal driving circuit generating a drain scanning signal for controlling the timing
of supplying a video signal to a plurality of the data lines,

10 wherein all the gate wirings in the vertical driving circuit or the horizontal driving circuit
in direct contact with only one corresponding active layer.